What is claimed is:

1. A semiconductor die assembly (200, 300, 400), comprising:

a plurality of die packages (100), each including:

a lead frame (10) having a plurality of leads (11) surrounding a central region (12), each of the leads (11) having a first surface (14) and a down set portion (101) extending from the first surface (14),

a semiconductor die (30) disposed in the central region (12) and electrically connected to the leads (11), the semiconductor die (30) having a first surface (34) formed thereon, the first surface (34) of the semiconductor die (30) being substantially coplanar with the first surface (14) formed on each of the leads (11), and

an encapsulant (50) disposed in the central region (12) and covering the semiconductor die (30) and a portion of the leads (11), the first surface (14) of the leads (11) and the first surface (34) of the semiconductor die (30) being exposed from the encapsulant (50), and the first surface (34) of the semiconductor die (30) and the down set portions (101) of the leads (11) forming a cavity (102);

wherein the plurality of die packages (100) are stacked such that at least a portion of the encapsulant (50) is disposed in the cavity (102) of a next higher die package (100) in the stack.

2. The semiconductor die assembly (200) of claim 1, wherein the leads (11) of a top die package (100) in the stack are down set further than the leads (11) of a lower die package (100) in the stack.

3. The semiconductor die assembly (300, 400) of claim 1, wherein the leads (11) of each die package (100) in the stack are of equal length.

4. The semiconductor die assembly (300, 400) of claim 1, wherein the lower surfaces of the down set portions (101) of at least one die package (100) in the stack is soldered to the upper surfaces of the down set portions (101) of an adjacent die package (100) in the stack.

5. The semiconductor die assembly (400) of claim 4, wherein solder balls (414) are attached to the down set portions (101) of the packages (100) prior to stacking the packages (100).

6. The semiconductor die assembly (300, 400) of claim 4, wherein the packages (100) in the stack are adhered together prior to being soldered.

7. The semiconductor die assembly (200, 300, 400) of claim 1, wherein the sides of the encapsulant (50) are tapered.

8. The semiconductor die assembly (200, 300, 400) of claim 1, wherein the plurality of leads (11) are disposed on two or more sides of the central region (12).

9. A method for forming a semiconductor die assembly (200, 300, 400), the method comprising:

forming a plurality of individual semiconductor die packages (100), including:

providing a lead frame (10) having a plurality of leads (11) surrounding a central region (12), each of the leads (11) including a first surface (14) formed thereon,

disposing a semiconductor die (30) in the central region (12), the semiconductor die (30) having a first surface (34) formed thereon, the first surface (34) of the semiconductor die (30) being substantially coplanar with the first surface (14) formed on each of the leads (11),

electrically connecting the semiconductor die (30) to the leads (11),

covering a portion of the semiconductor die (30) and a portion of the leads (11) with an encapsulant (50), and

shaping each of the leads (11) to include a first surface (14) and a down set portion (101) extending from the first surface (14), the first surface (14) of the leads and the first surface (34) of the semiconductor die (30) being exposed from

the encapsulant (50), and the first surface (34) of the semiconductor die (30) and the down set portions (101) of the leads (11) forming a cavity (102);

stacking the plurality of individual semiconductor die packages (100) such that at least a portion of the encapsulant (50) is disposed in the cavity (102) of a next higher semiconductor die package (100) in the stack; and

electrically interconnecting corresponding leads (11) of the stacked semiconductor die packages (100).

10. The method of claim 9, wherein the leads (11) of a top semiconductor die package (100) in the stack are down set further than the leads (11) of a lower semiconductor die package (100) in the stack.

11. The method of claim 9, wherein the leads (11) of each semiconductor die package (100) in the stack are of equal length.

12. The method of claim 9, wherein the electrically interconnecting includes:

soldering the lower surfaces of the down set portions (101) of at least one semiconductor die package (100) in the stack to the upper surfaces of the down set portions (101) of an adjacent semiconductor die package (100) in the stack.

13. The method of claim 12, further comprising:

attaching solder balls (414) to the down set portions (101) of the semiconductor die packages (100) prior to stacking the semiconductor die packages (100).

14. The method of claim 12, further comprising:

dipping the leads (11) in a solder bath.

15. The method of claim 14, further comprising:

adhering the semiconductor die packages (100) in the stack together prior to dipping.

16. The method of claim 9, wherein the sides of the encapsulant (50) are tapered.

17. The method of claim 9, wherein the plurality of leads (11) are disposed on two or more sides of the central region (12).

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18. The method of claim 9, further comprising,

adhering the semiconductor die packages (100) in the stack together prior to electrically interconnecting.

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